CLAIM LISTING

This listing of claims will replace all prior versions and listings of claims in the application:

AMENDMENTS TO THE CLAIMS:

With claims 1-37 originally pending, please cancel claims 15-18, 24 and 30-37. Further, please amend claims 19, 21, 25 and 28 as indicated in the list of claims to follow.

1. (Original) An integrated high-speed parallel-to-serial and serial-to-parallel transceiver, wherein the transceiver comprises:

receiver section that includes:

receiver clocking circuit operably coupled to produce at least one high frequency receiver clock;

serial to parallel module operably coupled to convert inbound serial data into inbound parallel data at a rate corresponding to the at least one high frequency receiver clock; and

receiver compensation operable to at least partially compensate for at least one of integrated circuit operational limitations and integrated circuit fabrication limitations of at least one of the receiver clocking circuit and the serial to parallel module;

transmitter section that includes:

transmitter clocking circuit operably coupled to produce at least one high frequency transmitter clock;

parallel to serial module operably coupled to convert outbound parallel data into outbound serial data at a rate corresponding to the at least one high frequency transmitter clock; and

transmitter compensation operable to at least partially compensate for at least one of the integrated circuit operational limitations and the integrated circuit fabrication limitations of at least one of the transmitter clocking circuit and the parallel to serial module.

2. (Original) The transceiver of claim 1, wherein the serial to parallel module and the receiver compensation further comprise:

an analog front end operably coupled to receive and amplify the inbound serial data to produce received inbound serial data;

even/odd splitter operably coupled to split the received inbound serial data into serial even data and serial odd data;

even serial to parallel converter operably coupled to convert the serial even data into parallel even data;

odd serial to parallel converter operably coupled to convert the serial odd data into parallel odd data; and

output interface operably coupled to output the parallel even data and the parallel odd data as the inbound parallel data.

3. (Original) The transceiver of claim 2, wherein the analog front end further comprises:

an interface;

an inductive amplifier operably coupled to the interface; and

a feed forward boost module operably coupled to the inductive amplifier.

4. (Original) The transceiver of claim 2, wherein each of the even and odd serial to parallel converters further comprises:

a plurality of interoperably coupled high-speed, low power, differential flip flops.

5. (Original) The transceiver of claim 1, wherein the receiver clocking circuit and the receiver compensation further comprise:

fine phase detector operably coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock;

fine charge pump operably coupled to produce a voltage representative of the fine difference signal;

coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock that is representative of the at least one high frequency receiver clock;

coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal;

filter operably coupled to filter the voltage representation of the coarse difference signal and the voltage representation of the fine difference signal to produce a filtered difference representation;

voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation;

post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency receiver clock;

coarse divider operably coupled to produce the coarse feedback clock from the at least one high frequency receiver clock.

6. (Original) The transceiver of claim 5, wherein the receiver clocking circuit and the receiver compensation further comprises:

duty cycle distortion correction module operably coupled to compensate for duty cycle distortion of a differential representation of the at least one high frequency clock.

7. (Original) The transceiver of claim 5, wherein the at least one high frequency receiver clock further comprises:

critical analog high frequency receiver clock;

analog high frequency receiver clock; and

digital high frequency receiver clock.

8. (Original) The transceiver of claim 1, wherein the parallel to serial module and the transmitter compensation further comprise:

interface operably coupled to receive the outbound parallel data;

even parallel to serial converter operably coupled to convert an even portion of the outbound parallel data into even serial outbound data;

odd parallel to serial converter operably coupled to convert an odd portion of the outbound parallel data into odd serial outbound data;

combiner operably coupled to combine the even serial outbound data and the odd serial outbound data into combined serial data; and

driver operably coupled to produce the outbound serial data from the combined serial data.

9. (Original) The transceiver of claim 8, wherein the interface further comprises:

differential input interface having a calibrated input impedance; and

buffer operably coupled to temporarily store the outbound parallel data received via the differential input interface.

10. (Original) The transceiver of claim 8, wherein each of the even and odd parallel to serial converters further comprises:

a plurality of interoperably coupled high-speed, low power, differential flip flops.

11. (Original) The transceiver of claim 1, wherein the transmitter clocking circuit and the transmitter compensation further comprise:

phase and frequency detector operably coupled to produce a difference signal based on a difference between a reference clock and a feedback clock that is representative of the at least one high frequency transmitter clock;

charge pump operably coupled to produce a voltage representative of the difference signal;

filter operably coupled to filter the voltage representation of the difference signal to produce a filtered difference representation;

voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation;

post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency transmitter clock;

and

divider operably coupled to produce the feedback clock from the at least one high frequency transmitter clock.

12. (Original) The transceiver of claim 11, wherein the transmitter clocking circuit and the transmitter compensation further comprises:

offset module operably coupled to provide DC offset compensation by modifying the filtered difference representation.

13. (Original) The transceiver of claim 11, wherein the transmitter clocking circuit and the transmitter compensation further comprise:

duty cycle correction module operably coupled to correct duty cycle of the at least one high frequency transmitter clock.

14. (Original) The transceiver of claim 13, wherein the transmitter clocking circuit and the transmitter compensation further comprise:

phase error correction circuit operably coupled to correct phase error of the at least one high frequency transmitter clock..

15-18. (Cancelled)

19. (Currently Amended) A high-speed parallel-to-serial and serial-to-parallel, wherein the transceiver comprises:

clocking circuit operably coupled to produce at least one high frequency clock;

serial to parallel module operably coupled to convert inbound serial data into inbound parallel data at a rate corresponding to the at least one high frequency clock;

parallel to serial module operably coupled to convert outbound parallel data into outbound serial data at a rate corresponding to the at least one high frequency clock; and

compensation operable to at least partially compensate for at least one of integrated circuit operational limitations and integrated circuit fabrication limitations of at least one of the clocking circuit, the parallel to serial module, and the serial to parallel module ~~The transceiver of claim 15~~, wherein the clocking circuit and the compensation further comprise:

fine phase detector operably coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock;

fine charge pump operably coupled to produce a voltage representative of the fine difference signal;

coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock that is representative of the at least one high frequency receiver clock;

coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal;

filter operably coupled to filter the voltage representation of the coarse difference signal and the voltage representation of the fine difference signal to produce a filtered difference representation;

voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation;

post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency receiver clock;

coarse divider operably coupled to produce the coarse feedback clock from the at least one high frequency receiver clock.

20. (Original) The transceiver of claim 19, wherein the clocking circuit and the compensation further comprises:

duty cycle distortion correction module operably coupled to compensate for duty cycle distortion of a differential representation of the at least one high frequency clock.

21. (Currently Amended) The transceiver of claim ~~15~~ 19, wherein the parallel to serial module and the compensation further comprise:

interface operably coupled to receive the outbound parallel data;

even parallel to serial converter operably coupled to convert an even portion of the outbound parallel data into even serial outbound data;

odd parallel to serial converter operably coupled to convert an odd portion of the outbound parallel data into odd serial outbound data;

combiner operably coupled to combine the even serial outbound data and the odd serial outbound data into combined serial data; and

driver operably coupled to produce the outbound serial data from the combined serial data.

22. (Original) The transceiver of claim 21, wherein the interface further comprises:

differential input interface having a calibrated input impedance; and

buffer operably coupled to temporarily store the outbound parallel data received via the differential input interface.

23. (Original) The transceiver of claim 22, wherein each of the even and odd parallel to serial converters further comprises:

a plurality of interoperably coupled high-speed, low power, differential flip flops.

24. (Cancelled)

25. (Currently Amended) An integrated high-speed serial-to-parallel receiver, wherein the receiver comprises:

clocking circuit operably coupled to produce at least one high frequency clock;

serial to parallel module operably coupled to convert inbound serial data into inbound parallel data at a rate corresponding to the at least one high frequency clock; and

compensation operable to at least partially compensate for at least one of integrated circuit operational limitations and integrated circuit fabrication limitations of at least one of the clocking circuit and the serial to parallel module ~~The receiver of claim 24~~, wherein the serial to parallel module and the compensation further comprise:

an analog front end operably coupled to receive and amplify the inbound serial data to produce received inbound serial data;

even/odd splitter operably coupled to split the received inbound serial data into serial even data and serial odd data;

even serial to parallel converter operably coupled to convert the serial even data into parallel even data;

odd serial to parallel converter operably coupled to convert the serial odd data into parallel odd data; and

output interface operably coupled to output the parallel even data and the parallel odd data as the inbound parallel data.

26. (Original) The receiver of claim 25, wherein the analog front end further comprises:

an interface;

an inductive amplifier operably coupled to the interface; and

a feed forward boost module operably coupled to the inductive amplifier.

27. (Original) The receiver of claim 25, wherein each of the even and odd serial to parallel converters further comprises:

a plurality of interoperably coupled high-speed, low power, differential flip flops.

28. (Currently Amended) The receiver of claim ~~24~~ 25, wherein the clocking circuit and the compensation further comprise:

fine phase detector operably coupled to produce a fine difference signal based on a phase difference between the inbound serial data and a fine feedback clock that is representative of the at least one high frequency receiver clock;

fine charge pump operably coupled to produce a voltage representative of the fine difference signal;

coarse phase and frequency detector operably coupled to produce a coarse difference signal based on a difference between a reference clock and a coarse feedback clock that is representative of the at least one high frequency receiver clock;

coarse charge pump operably coupled to produce a voltage representative of the coarse difference signal;

filter operably coupled to filter the voltage representation of the coarse difference signal and the voltage representation of the fine difference signal to produce a filtered difference representation;

voltage controlled oscillator operably coupled to produce an oscillation based on the filtered difference representation;

post PLL filter operably coupled to amplify and filter the oscillation to produce the at least one high frequency receiver clock;

coarse divider operably coupled to produce the coarse feedback clock from the at least one high frequency receiver clock.

29. (Original) The receiver of claim 28, wherein the clocking circuit and the compensation further comprises:

duty cycle distortion correction module operably coupled to compensate for duty cycle distortion of a differential representation of the at least one high frequency clock.

30-37. (Cancelled)